REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1, 3-5, 8-11, 13-15, 17-25, and 27-29 are pending in the application. The Examiner additionally stated that claims 1, 3-5, 8-11, 13-15, 17-25, and 27-29 are rejected. By this amendment, claims 1, 11, and 21 are amended. Hence, claims 1, 3-5, 8-11, 13-15, 17-25, and 27-29 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Claims

Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claims 1, 11, and 21 under 35 U.S.C. 103(a) as being unpatentable over the background of the specification in view of Philip, U.S. Patent No. 3,130,387 (hereinafter, "Philip"). Applicant respectfully traverses the Examiner's rejections.

The Examiner noted that the background of the instant application specification teaches a microprocessor apparatus, for precluding a pipeline stall due to microcode ROM access delay, the microprocessor apparatus comprising:

- a translator, configured to generate a plurality of micro instructions corresponding to an instruction and a microcode entry point (Spec: 0007);
- early access logic, couple to said translator, configured to employ said microcode entry point to access a microcode ROM prior to when said microcode entry point is provided to register logic, whereby said microcode ROM provides a first micro instruction to said register logic when said first micro instruction is required by said register logic, and wherein said translator provides said plurality of micro instructions to said register logic (Spec: 0009) (The Examiner stated that all of this inherently flows from the specification and that it would be inefficient to have another unit generate the ROM address when the translator is already determining what the instruction is.); and

- a microcode ROM, configured to provide a second part of a micro instruction sequence corresponding to said microcode entry point (Spec 0009).

The Examiner stipulated that the only aspect that is not taught by the specification is a buffer between the translator and the register logic and that the inventors have identified the problem that exists in the dual translation process described in 0009 of the specification is that the translator and the ROM can get out of synchronization because of delay caused by a larger ROM. The Examiner opined that the problem described is a very old one that has been resolved long ago (Philip: Title), and that one of ordinary skill in the pertinent art would have readily realized that when two independent data producing objects become unsynchronized, that a buffer may be implemented.

The Examiner rejected claims 11 and 21 for the same reasons.

In reply, Applicant notes that claims 1, 11, and 21, as amended herein, each recite:

- early access logic, coupled to said micro instruction queue, configured to employ a selected microcode entry point from a selected one of said plurality of micro instruction queue entries to access said microcode ROM prior to when said selected microcode entry point is provided to said register logic, whereby said microcode ROM provides a first one of second micro instructions to said register logic when said first one is required by said register logic, and wherein said early access logic employs said selected microcode entry point when said selected microcode entry point is positioned within said micro instruction queue a number of entries prior to transfer to said register logic that is equal to the number of excess clock cycles exhibited by the microcode ROM access delay over that already compensated for by configuration of said translator and said micro instruction queue.

Early access logic, which functions as noted above, is not disclosed nor suggested by the background, Phillip, or a combination of the background and Phillip.

Accordingly, it is requested that the rejections of claims 1, 11, and 21 be withdrawn.

The Examiner also rejected claims 1, 3-5, 8-11, 13-15 and 17-25, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carbine et al. (US Patent 5,222,244) (hereinafter, "Carbine), in view of the background of the specification. Applicant respectfully traverses the rejections.

As per claim 1, the Examiner noted that Carbine teaches a microprocessor apparatus, for precluding a pipeline stall due to microcode ROM access delay, the microprocessor apparatus comprising:

- a plurality of micro instruction queue entries, each corresponding to an instruction, and said each comprising a plurality of micro instructions and a microcode entry point (column 6, lines 58-68; column 7, lines 1-19);
- early access logic, coupled to said micro instruction queue, configured to employ said microcode entry point to access a microcode ROM prior to when said microcode entry point is provided to register logic, whereby said microcode ROM provides a first micro instruction to said register logic when said first micro instruction is required by said register logic (column 8, lines 39-46); and
- a microcode ROM, configured to provide a second part of a micro instruction sequence corresponding to said microcode entry point (column 7, lines 17-1 9; column 8, lines 39-46).

The Examiner stated that Carbine does not teach the microprocessor apparatus comprising:

- a translator, coupled to said plurality of micro instruction queue entries, configured to generate said microcode instruction queue entry (column 6, lines 58-68; column 7, lines 1-19);

and that Carbine does not disclose how the contents of the queue entries are determined, but that Applicant has disclosed as prior art that the combination of a microcode ROM and a direct translator for the sequencing of macroinstructions is known in the art.

The Examiner noted that the combination of the microcode ROM and a direct translator in coordination with the microcode queue would be a viable, beneficial solution in

Carbine, and further pointed out that an opposing possibility would be to statically populate the queue with the most commonly used instructions. The Examiner stated that one of ordinary skill in the pertinent art would have recognized that this would not be extremely useful because it would only provide the benefits of not stalling on a microcode ROM instruction in the instance of encountering a common instruction, which might not extend across different applications, and that, in contrast, a queue that is dynamically populated by a translator when the microcode ROM instruction is first encountered will provide the benefits of the invention to all microcode ROM instructions.

The Examiner thus concluded that it would have been obvious to one of ordinary skill in the pertinent art at the time of the invention that providing a translator to generate the microinstruction queue entries in Carbine would provide the benefit of not stalling on any microcode ROM instruction, rather than a select few, and that it is inherent that that translator will generate the micro instruction queue entries in order, since the translate requests would be sent to it in order and the register logic would need the entry in order.

The Examiner noted that what cannot be inferred by this combination, however, is that said early access logic employs said microcode entry point when it is within a bottom micro instruction queue entry, said bottom micro instruction queue entry comprising one of said each, and wherein said bottom micro instruction queue entry will be provided to said register logic during a next clock cycle. The Examiner noted that this is because there is no evidence that Carbine's microcode translation ROM is a FIFO queue and that the combination suggested could very well just put the next entry in the first available slot.

However, the Examiner pointed out since it has been established that the entries would have to be provided to the register logic in the order that they were created, this would mean that each entry would need a tag associated with it, numbered to correspond to when it was entered into the queue, and that one of ordinary skill in the pertinent art however will realize that this creates some obstacles. The Examiner further noted that comparing tags in any unstructured (i.e. randomly ordered) storage area is time consuming, and that the extra field required to mark all of the entries also uses up space

and wastes power, but on the other hand, keeping the entries in order means only having to check one register to see where the head of the queue is quick and easy. Consequently, the Examiner concluded that one of ordinary skill in the pertinent art would be motivated to use a structured FIFO queue rather than a random queue.

Applicant respectfully disagrees with the Examiner's characterization of the teachings of Carbine and of the background of the specification and offers the following arguments in traversal. First, claim 1, as amended herein, is provided below for ease of reference.

1. A microprocessor apparatus, for precluding a pipeline stall due to microcode ROM access delay, the microprocessor apparatus comprising:

a translator, configured to generate a plurality of micro instruction queue entries, each of said plurality of micro instruction queue entries corresponding to an instruction, and said each of said plurality of micro instruction queue entries comprising a plurality of micro instructions and a microcode entry point, wherein said translator generates said each of said plurality of micro instruction queue entries in order;

a micro instruction queue, coupled to said translator, configured to receive said each of said plurality of micro instruction queue entries in said order, and configured to provide said each of said plurality of micro instruction queue entries to register logic in said order;

a microcode ROM, configured to provide a second part of a micro instruction sequence corresponding to said microcode entry point; and

early access logic, coupled to said micro instruction queue, configured to employ a selected microcode entry point from a selected one of said plurality of micro instruction queue entries to access said microcode ROM prior to when said selected microcode entry point is provided to said register logic, whereby said microcode ROM provides a first micro instruction from said second part to said register logic when said first micro instruction is required by said register logic, and wherein said early access logic employs said selected microcode entry point when said selected microcode entry point is positioned within said micro instruction queue a number of entries prior to transfer to said register logic that is equal to the number of excess clock cycles exhibited by the microcode ROM access delay over that already compensated for by configuration of said translator and said micro instruction queue.

Note that claim 1, in combination with other elements and limitations, recites both a translator and a microcode ROM. Clearly, the background teaches these elements. But neither Carbine nor the background teach:

- early access logic, coupled to said micro instruction queue, configured to employ a selected microcode entry point from a selected one of said plurality of micro instruction queue entries to access said microcode ROM prior to when said selected microcode entry point is provided to said register logic, whereby said microcode ROM provides a first micro instruction from said second part to said register logic when said first micro instruction is required by said register logic, and wherein said early access logic employs said selected microcode entry point when said selected microcode entry point is positioned within said micro instruction queue a number of entries prior to transfer to said register logic that is equal to the number of excess clock cycles exhibited by the microcode ROM access delay over that already compensated for by configuration of said translator and said micro instruction queue.

Accordingly, in view of the arguments submitted above, Applicant requests that the rejection of claim 1 be withdrawn.

Claims 3-5 depend from claim 1 and add further limitations over that which has been argued as being allowable over the noted references and it is accordingly requested that the rejections be withdrawn.

Claim 11 recites substantially the same elements as have been argued above as being allowable over the noted references. Therefore, Applicant respectfully requests that the rejection of claim 11 be withdrawn as well.

Claims 13-15 and 17-20 depend from claim 11 and add further limitations over that which has been argued as being allowable over the noted references and it is accordingly requested that the rejections be withdrawn.

Claim 21 recites substantially the same elements as have been argued above as being allowable over the noted references. Therefore, Applicant respectfully requests that the rejection of claim 21 be withdrawn as well.

Claims 22-25 and 27-29 depend from claim 21 and add further limitations over that which has been argued as being allowable over the noted references and it is accordingly requested that the rejections be withdrawn.

CONCLUSIONS

In view of the arguments advance above, Applicant respectfully submits that claims 1, 3-5, 8-11, 13-15, 17-25, and 27-29 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

I hereby certify under 37 CFR 1.8 that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date of signature shown below.

Respectfully submitted,
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